**DAILY ASSESSMENT FORMAT**

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| **Date:** | **10-June-2020** | **Name:** | **Raziya Banu** |
| **Course:** | **VLSI** | **USN:** | **4AL16EC058** |
| **Topic:** | **MOS transistor basics-I** | **Semester & Section:** | **8th sem & ‘B’ section** |
| **Github Repository:** |  |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report –**  In my first session today I have studied about the MOSFET - MOS transistor basics-I  **INTRODUCTION TO THE MOSFET**  The two PN junctions are the source and the drain that supplies the electrons or holes to the transistor and drains them away respectively. The name field-effect transistor or FET refers to the fact that the gate turns the transistor (inversion layer) on and off with an electric field through the oxide. A transistor is a device that presents a high input resistance to the signal source, drawing little input power, and a low resistance to the output circuit, capable of supplying a large current to drive the circuit load.  The silicon surfaces under the thick isolation oxide have very high threshold voltages and prevent current flows between the N+ (and P+) diffusion regions along inadvertent surface inversion paths in an IC chip. Figure 6–1 also shows the MOSFET IV characteristics. Depending on the gate voltage, the MOSFET can be off (conducting only a very small off-state leakage current, Ioff) or on (conducting a large on-state current, Ion).  The gate voltage determines whether a current flows between the drain and source or not. Gate Oxide Drain Idrain Vdrain Source P Semiconductor body N N Ion Vg 1.8 V Vg 0 Ioff (a) (b) (b) Switch representation Drain Gate Source (a) Circuit symbol Drain Gate Source  ● Early Patents on the FET  ● The transistor and IC technologies owe their success mainly to the effort and ingenuity of a large number of technologists since the mid-1900s.    Two early FET patents are excerpted here. These earliest patents are presented for historical interest only. Many more conceptual and engineering innovations and efforts were required to make MOSFETs what they are today. J. E. Lilienfeld’s 1930 U.S. patent is considered the first teaching of the FET. 11 and 12 are metal contacts to the source and drain. 15 is a thin film of semiconductor (copper sulfide). Lilienfeld taught the following novel method of making a small (short) gate, the modern photolithography technique being yet unavailable to him.  ● Introduction to the MOSFET 197 and then reassembled (glued back) with a thin aluminum foil inserted between the two pieces.  The edge of the Al foil is used as the gate. The semiconductor film is deposited over the glass substrate and the gate, and source and drain contacts are provided. There is no oxide between the gate electrode and the semiconductor. The insulator in this FET would be the depletion layer at the metal–semiconductor junction (see Section 6.3.2). “A perspective view, on a greatly enlarged scale and partly in section, of the novel apparatus as embodied by way of example in an amplifier.” In a 1935 British patent, Oskar Heil gave a lucid description of a MOSFET. Referring to Fig. 6–4, “1 and 2 are metal electrodes between which is a thin layer 3 of semiconductor. A battery 4 sends a current through the thin layer of semiconductor and this current is measured by the ammeter 5. If, now, an electrode 6 in electro-static association with the layer 3 is charged positively or negatively in relation to the said layer 3, the electrical resistance of this layer is found to vary and the current strength as measured by the ammeter 5 also to vary.”  ● MOS Transistor 6.2 COMPLEMENTARY MOS (CMOS) TECHNOLOGY Modern MOSFET technology has advanced continually since its beginning in the 1950s. It shows the poly-Si gate and the single-crystalline Si body with visible individual Si atoms and a 1.2 nm amorphous SiO2 film between them. 1.2 nm is the size of four SiO2 molecules. The basic steps of fabricating the MOSFET shown in Fig. 6–1 is to first make shallow-trench-isolation by etching a trench that defines the boundary of the transistor and filling the trench with chemical vapor deposition (CVD) oxide .Next, planarize the wafer with CMP (see Section 3.8), grow a thin layer of oxide (gate oxide) over the exposed silicon surface, deposit a layer of polycrystalline silicon as the gate material , use optical lithography to pattern a piece of photoresist, and use the photoresist as a mask to etch the poly-Si to define the gate . Finally, implant As into the source and drain. The implantation is masked by the gate on one side and the trench isolation on the other. Rapid thermal annealing (see text box in Section 3.6) is applied to activate the dopant and repair the implantation damage to the crystal. Contacts can then be made to the source, drain, and the gate. Figure 6–6a is an N-channel MOSFET, or N-MOSFET or simply NFET. In both cases, Vg and Vd swing between 0 V and Vdd, the power-supply voltage. The body of an NFET is connected to the lowest voltage in the circuit, 0 V, as shown in (b).  Consequently, the PN junctions are always reverse-biased or unbiased and do not conduct forward diode current. When Vg is equal to Vdd as shown in (b), an inversion layer is present and the FIGURE 6–5 Gate oxides as thin as 1.2 nm can be manufactured reproducibly. Individual Si atoms are visible in the substrate and in the polycrystalline gate. (The example is an inverter. It charges and discharges the output node with its load capacitance, C, to either Vdd or 0 under the command of Vg. When Vg = Vdd, the NFET is on and the PFET is off (think of them as simple on–off switches), and the output node is pulled down to the ground (Vout = 0). When Vg = 0, the NFET is off and the PFET is on; the output node is pulled up to Vdd. In either static case, one of the two transistors is off and there is no current flow from Vdd through the two transistors directly to the ground. Therefore, CMOS circuits consume much less power than other types of circuits. Figure 6–7b illustrates how NFET and PFET can be fabricated on the same chip. Portions of the P-type substrate are converted into N-type wells by donor implantation and diffusion. Contacts to the P substrate and N well are included in the figure. |

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| **Course:** | **Udemy** | **USN:** | **4AL16EC058** | |
| **Topic:** | **Programming core Java** | **Semester & Section:** | **8th sem & ‘B’ section** | |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session** | | | |
| **While Loops** In the fourth part of the Java tutorial for beginners video series using Eclipse, we look using loops to make your code repeat statements multiple times. We also take a look at conditions.  **public** **class** **Application** **{**  **public** **static** **void** **main(**String**[]** args**)** **{**    **int** value **=** 0**;**    **while(**value **<** 10**)**  **{**  System**.**out**.**println**(**"Hello " **+** value**);**    value **=** value **+** 1**;**  **}**  **}**  **}**    Hello 0  Hello 1  Hello 2  Hello 3  Hello 4  Hello 5  Hello 6  Hello 7  Hello 8  Hello 9 **For Loops** In the fifth part of the Java tutorial for beginners video series using Eclipse, we look using 'for' loops and printf().  **public** **class** **Application** **{**  **public** **static** **void** **main(**String**[]** args**)** **{**    **for(int** i**=**0**;** i **<** 5**;** i**++)** **{**  System**.**out**.**printf**(**"The value of i is: %dn"**,** i**);**  **}**  **}**  **}**    The value of i is: 0  The value of i is: 1  The value of i is: 2  The value of i is: 3  The value of i is: 4 | | | |